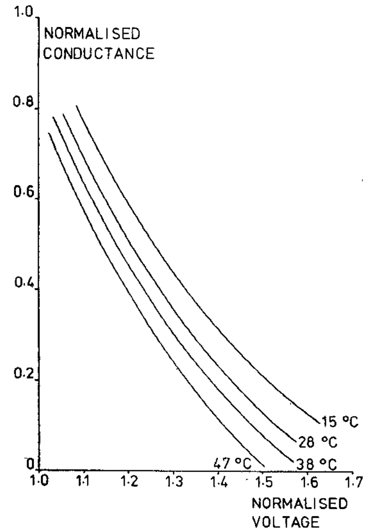

Fig. 9. Variation of conductance with temperature for Gunn diode.

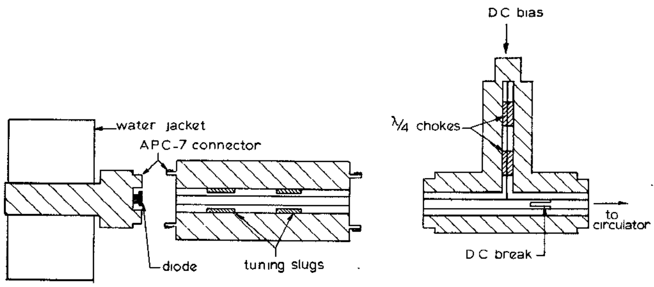

Fig. 10. Test cavity for IMPATT diodes.

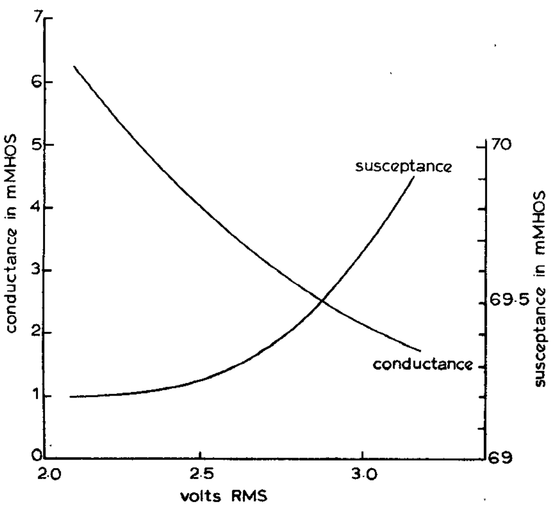

Fig. 11. Dynamic conductance and susceptance for IMPATT diode.

DISCUSSION

This method of device characterization has several advantages over other methods.

The device under test is operated as an oscillator near to its normal working point. This eliminates problems of device stabilization which are encountered with some other methods.

The variation in the locking signal amplitude appears to the device as a change in the complex admittance which it "sees." Thus the method is comparable with other techniques in which the load admittance is physically altered. Advantages of the present method are that the frequency remains independent of the load condition, and that the RF voltage at the diode is controllable. The method is relatively fast and amenable to automation.

The relative measurements can all be made without physically disturbing the cavity. This is important in the case of small changes in the diode admittance, e.g., when the dc bias is changed, since they may often be obscured by the results of mechanical disturbance.

With this method, results can only be obtained over a limited range of diode RF voltage. However, this range is in the region in which the diode is usually operated.

The accuracy of this method of diode characterization is affected by several factors, the most important being the following.

1) Inaccuracies in the measurement of the free-running diode admittance. These are due to the physical disturbance of the cavity required to make the measurement and to the subsequent alteration of the field pattern near the diode site.

2) Errors in the relative measurement of conductance against voltage (and susceptance against voltage). These are mainly due to difficulty in estimating a line of symmetry for the phase-gain curves, which is required for the 0° phase reference.

3) Changes produced in the voltage and current waveforms at the diode, due to the presence of the large locking signal. The voltage and current waveforms in a Gunn diode oscillator have been examined under large-signal injection-locking conditions. The harmonic content which is of the order of 10 percent is not greatly influenced by the introduction of a locking signal.

An error is introduced in the calibration procedure when the test cavity is replaced by a short circuit. The error arises from the difference in the electrical length between the cavity and the short circuit, and, for the frequency deviations used, is less than 3 percent.

A correction may be made from a calibration taken with a short circuit placed at the diode site. This calibration may also be used to correct for nonlinearities in the phase-frequency response of the cavity coupling system.

Typical measured values for the deviation from a linear phase-frequency response account for an error of 1 percent.

The overall measurement accuracy is estimated to be better than ±20 percent.

REFERENCES

[1] J. P. Quine, "Injection phase-locking characteristics of LSA-mode transferred-electron oscillators," *Proc. IEEE* (Lett.), vol. 57, pp. 715–717, Apr. 1969.
[2] M. Michaelides and I. M. Stephenson, "Injection locking of microwave solid-state oscillators," *Proc. IEEE* (Lett.), vol. 59, pp. 319–321, Feb. 1971.
[3] R. Adler, "A study of locking phenomena in oscillators," *Proc. IRE*, vol. 34, pp. 351–357, June 1946.
[4] L. J. Paciorek, "Injection locking of oscillators," *Proc. IEEE*, vol. 53, pp. 1723–1727, Nov. 1965.
[5] R. P. Owens and D. Cawsey, "Microwave equivalent-circuit parameters of Gunn-effect-device packages," *IEEE Trans. Microwave Theory Tech.* (*Special Issue on Microwave Circuit Aspects of Avalanche-Diode and Transferred Electron Devices*), vol. MTT-18, pp. 790–798, Nov. 1970.
[6] H. L. Hartnagel and M. Kawashima, "Negative TEO-diode conductance by transient measurement and computer simulation," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-21, pp. 468–477, July 1973.

Designing Microstrip Matching Networks for Microwave-Transistor Power Amplifiers

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***Abstract*—A computer-aided design procedure is formulated for *L*-band-transistor power amplifiers. The procedure incorporates a precision measurement technique for transistor impedances, a model for large step discontinuities in microstrip, and an optimization routine for the direct realization of broad-band matching circuits.**

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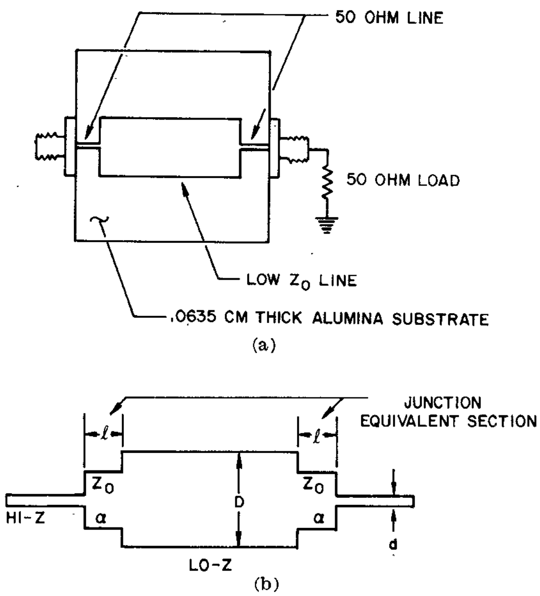

Fig. 1. (a) Experimental hardware. (b) Junction equivalent section.

INTRODUCTION

In recent years considerable effort has been extended in the area of the design of class-C microwave-transistor power amplifiers. The material contained herein outlines a procedure for the specification, optimization, and realization of the microstrip-matching circuits associated with transistor power amplifiers. The procedure incorporates a precision measurement technique for transistor impedances, a model for large step discontinuities in microstrip, and an optimization routine for the direct realization of broad-band matching circuits. The final computer outputs are the physical dimensions for microstrip transmission-line matching sections.

The transistor and circuit impedances used in this work are measured with a Hewlett-Packard manual network analyzer. Because the inherent errors of the analyzer could obscure the very low-level impedances encountered, a correction routine similar to that presented by Hand [1] is used. The method minimizes the test-equipment errors by correcting the measured values of the reflection coefficient, using error signals previously determined from measurements of precision offset shorts [2]. An estimated accuracy of the measurement of the reflection coefficients near unity is ± 0.005 and $\pm 1°$. Accuracies of this nature are required for the realization of the broad-band power-transistor matching sections.

The matching circuits, which consist of sections of transmission line in microstrip, often involve very large-impedance step discontinuities. Some earlier papers have considered the problem of small step discontinuities, but the results were found not to be applicable to very large steps [3]. Several circuits of different step sizes, similar to that shown in Fig. 1(a), have been constructed, and impedance measurements have been made in the 1–2-GHz region.

A lossy line section, as shown in Fig. 1(b), was chosen to model the large junction effects. A computer-optimization program adjusted the attenuation factor, characteristic impedance, and length of the junction-model sections so that the computed input impedance to the test line was the same as that measured over the full octave of 1–2 GHz. Good agreement has been obtained between computed and measured input impedances to complex multistep networks when the junction effects are taken into account.

The junction model presented has been used for 0.0635-cm alumina substrates with a relative dielectric constant of 10.4, and has been determined to be accurate in the 1–2-GHz region.

The transistor impedances used during this design procedure are measured by a circuit-substitution method. The transistors are configured as common-base class-C amplifiers and are installed in a transistor test fixture. The test fixture consists of a transistor-mounting section and two alumina substrates with 50-Ω transmission lines. Bias is applied through low-resistance coils, independent of the microstrip networks.

The 50-Ω line sections are overlayed with conductive tape as matching sections at several discrete frequencies. The overlays are adjusted until the desired performance characteristics are obtained at a single frequency; the test fixture is then disassembled and the circuit impedance measured. The procedure is repeated for several frequencies in the band of interest.

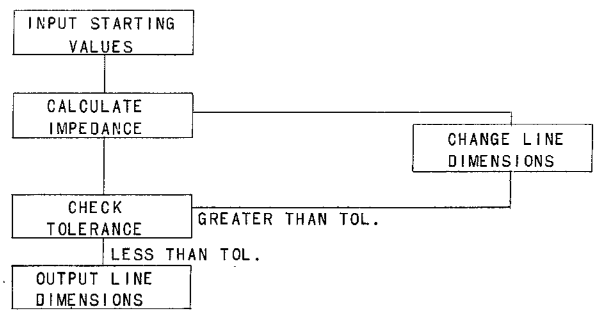

Fig. 2. Optimization routine block diagram.

CIRCUIT DESIGN

An optimization routine has been formulated which incorporates the step-discontinuity model and which requires the transistor impedances and starting values for the line dimensions as input. The approximate starting values are selected using conventional transmission-line matching-circuit theory [4], and the line dimensions are computer varied until the desired circuit impedances are obtained. The program produces the physical dimensions of the microstrip matching sections corrected for the impedance step discontinuities. A block diagram for the program is shown in Fig. 2.

RESULTS

The measured performance of an amplifier designed using the aforementioned procedure, and utilizing an MSC 2010 packaged transistor, is shown in Fig. 3(a). The results are compared with several other amplifiers using the same transistor that have been designed by conventional experimental methods. The performance of the computer-aided-designed amplifier is that obtained with no experimental network adjustment.

The results for another amplifier, which uses a PH1520A transistor, are shown in Fig. 3(b). The design criterion for this amplifier was to maintain a 28-W level across a 300-MHz band. The calculated results were based on passive network equations since the collector

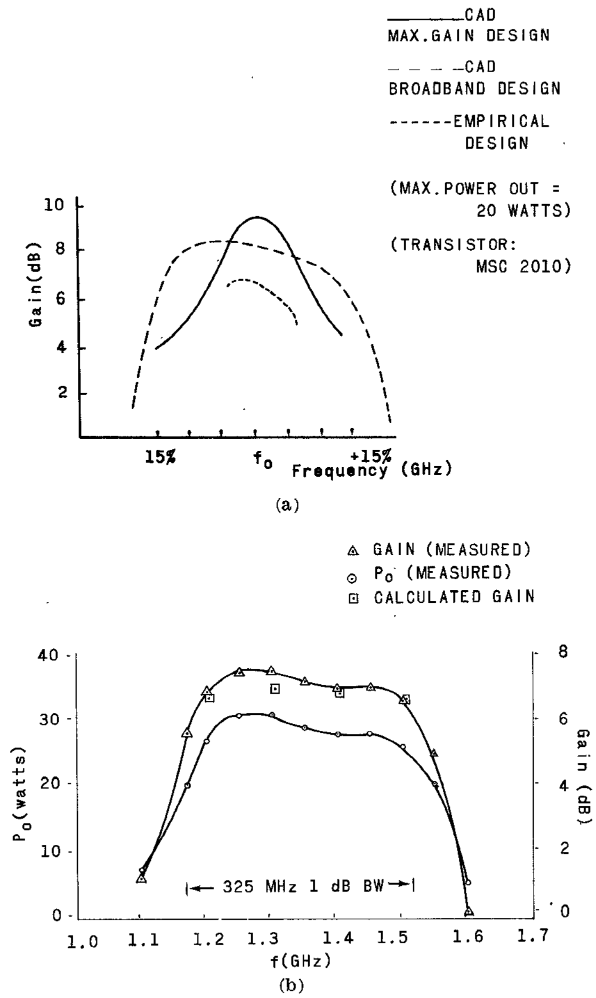

Fig. 3. (a) MSC 2010 CAD amplifier. (b) PH1520A CAD amplifier.

mismatch was rather modest (VSWR less than 1.4 with respect to maximum power operation). The total time required for the design, fabrication, and test of these amplifiers was less than one week each, and they required no experimental adjustments to meet the design criteria.

Subsequent effort will be applied to achieving the same degree of precision in the generation of matching networks for individual cells of multicell transistors. Methods will be sought for the generation of high-precision electrically reproducible networks for multicell matching (not necessarily lumped circuits), to minimize unit-to-unit variations in performance. Also, the intrinsic bandwidth limitations of various manufacturers' unit cells will be investigated to establish the degree of network complexity required to fully utilize the transistor's capability.

ACKNOWLEDGMENT

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REFERENCES

[1] B. P. Hand, "Developing accuracy specifications for automatic network analyzer systems," *Hewlett-Packard J.*, vol. 21, p. 16, 1970.

[2] G. T. O'Reilly and R. E. Neidert, "Computer program for increasing the accuracy of impedance measurements performed with a Hewlett-Packard manual network analyzer," Naval Res. Lab., Washington, D. C., NRL Memo. Rep. 2676, Nov. 1973.

[3] R. E. Neidert and G. T. O'Reilly, "Very large impedance steps in microstrip," *IEEE Trans. Microwave Theory Tech.* (Short Papers), vol. MTT-22, pp. 808–810, Aug. 1974.

[4] G. Matthaei, L. Young, and E. M. T. Jones, *Microwave Filters, Impedance-Matching Networks, and Coupling Structures.* New, York: McGraw-Hill, 1964.

X-Band TRAPATT Amplifier

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***Abstract*—The design and performance of broad-band TRAPATT amplifiers in *X* band are described along with a discussion of critical circuit parameters. Bandwidths of 10 percent and peak powers up to 38 W have been achieved using coaxial circuits with single and multichip diodes.**

INTRODUCTION

Wide-band TRAPATT amplifiers have been reported at frequencies between 1 and 5 GHz with bandwidths up to 15 percent [1]–[4]. At higher frequencies TRAPATT amplification has been achieved using an injection-locked oscillator [5], but no wide-band stable amplifier operation has been reported. This short paper describes an *X*-band pulsed TRAPATT amplifier which has demonstrated bandwidths of 10 percent with 5-dB gain. The design of the coaxial amplifier is described along with performance data on five units. Data are included for amplifiers utilizing stacked mesa diodes (higher peak power) and for ring diodes on diamond heat spreaders (improved thermal characteristics).

CIRCUIT DESCRIPTION

The coaxial amplifier circuit consists of the diode package and mount, a length of transmission line, a low-pass filter, and three tuning slugs. A cross-sectional drawing of the amplifier structure, which is similar to the *S*-band amplifier of [1], is shown in Fig. 1.

A five-section Chebyshev low-pass filter with a cutoff frequency of approximately 12 GHz was designed for the 0.162-in-diameter coaxial line. The filter, which consists of a series of alternating low- and high-impedance sections of transmission line machined on the center conductor, was fitted with a Teflon sleeve for support in the coaxial line. To adjust the phase of the harmonics reflected from the filter, the amplifier was constructed initially with spring fingers on the center conductor so that location of the filter relative to the diode could be optimized experimentally. The type of low-pass filter characteristic utilized in the amplifier does not appear critical, provided that adjustment of the filter spacing with respect to the diode is available.

Three 16.5-Ω slugs of varying lengths were positioned on the output side of the low-pass filter and were used to tune the amplifier response by adjustment of the load impedance at the fundamental frequency. These slugs had little effect on the loading at harmonic frequencies because of the low-pass filter. The principal effect of the three slugs was to smooth the amplifier passband; very little effect on the frequency of operation or bandwidth was observed.

The amplifier center frequency was adjusted by varying the corner inductance of the diode mount. This adjustment was accomplished with a series of tuning rings having various inner diameters as shown in Fig. 1.

In order to suppress oscillations in the amplifier, adjustment of the diode package parasitics was found necessary. Time domain computer simulations of the type reported by Carroll and Crede [6] for TRAPATT oscillators were performed to study the effect of variations in these parasitics for amplifiers. In these simulations the diode was represented by a current pulse generator in shunt with the diode depletion layer capacitance. The pulse generator represents the large, short duration current pulse induced by the charge carriers generated by the avalanche multiplication. This diode equivalent circuit was used in conjunction with a circuit model to compute in the time domain the diode voltage. The diode voltage was then analyzed for compatibility with the TRAPATT mode.

To establish confidence in the usefulness of this type of simulation, the load impedance of a TRAPATT oscillator was carefully measured using an automatic network analyzer and was used in the simulation

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